Amendments to the Claims

Claim 1 (previously amended): A ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode to said second gate electrode.

Claim 2 (original): The ferroelectric transistor according to claim 1, wherein:

said second gate intermediate layer includes two substructures configured mirror-symmetrically in relation to said first gate intermediate layer;

said second gate electrode includes two substructures configured mirror-symmetrically in relation to said first gate intermediate layer; and

said two substructures of said second gate electrode are electrically connected to each other.

Claim 3 (original): The ferroelectric transistor according to claim 2, wherein said first gate intermediate layer includes a dielectric layer configured between said surface of said semiconductor substrate and said ferroelectric layer.

Claim 4 (original): The ferroelectric transistor according to claim 1, wherein said first gate intermediate layer includes a dielectric layer configured between said surface of said semiconductor substrate and said ferroelectric layer.

Claim 5 (original): The ferroelectric transistor according to claim 4, wherein said dielectric layer of said first gate intermediate layer and said dielectric layer of said second gate intermediate layer are formed as a continuous dielectric layer.

Claim 6 (original): The ferroelectric transistor according to claim 1, comprising a diode structure connecting said first gate electrode to said second gate electrode, said diode structure including an electrode selected from the group consisting of said first gate electrode and said second gate electrode.

Claim 7 (original): The ferroelectric transistor according to claim 5, wherein;

said first gate electrode includes polycrystalline silicon including doping of a first conductivity type;

said second gate electrode includes polycrystalline silicon including doping of a second conductivity type that is opposite said first conductivity type; and

said first gate electrode adjacent said second gate electrode.

Claim 8 (previously amended): The ferroelectric transistor according to claim 1, comprising an auxiliary layer disposed between said ferroelectric layer and said first gate electrode.

Claim 9 (original): The ferroelectric transistor according to claim 1, wherein:

said first gate intermediate layer includes a material selected from the group consisting of CeO_2, ZrO_2, Y_2O_3, and $SrTiO_3$;

said second gate intermediate layer includes a material selected from the group consisting of SiO_2, CeO_2, ZrO_2, and $SrTiO_3$;

said ferroelectric layer includes a material selected from the group consisting of strontium-bismuth-tantalum, lead-zirconium- titante, lithium-niobate and barium-strontium-titanate; and

said semiconductor substrate includes monocrystalline silicon.

Claim 10 (original): The ferroelectric transistor according to claim 1, wherein said first gate electrode and said second gate electrode form a diode structure.

Claim 11 (previously amended): A memory cell configuration including a plurality of memory cells, each one of said plurality of said memory cells including a ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode to said second gate electrode.

Claim 12 (original): The memory cell configuration according to claim 11, comprising:

a plurality of bit lines, a plurality of supply lines, and a plurality of word lines crossing said plurality of said supply lines and said plurality of said bit lines;

each one of said plurality of said memory cells including a selection transistor connected between said second gate electrode of said ferroelectric transistor of the one of said plurality of said memory cells and one of said plurality of said supply lines, said selection transistor of each one of said memory cells including a control electrode connected to one of said plurality of said word lines; and

said ferroelectric transistor of each one of said plurality of said memory cells connected between adjacent ones of said plurality of said bit lines.

Claim 13 (currently amended): A method of producing a ferroelectric transistor according to claim 1, which comprises:

providing a semiconductor substrate with a surface;

applying, to the surface of the semiconductor substrate, a dielectric layer and a ferroelectric layer to provide a first intermediate layer, and a first electrode layer;

structuring the first electrode layer and the ferroelectric layer together to produce a first gate electrode, thereby

leaving the dielectric layer to provide a second intermediate layer;

applying and structuring a second electrode layer to produce a second gate electrode adjacent and laterally overlapping the first gate electrode; and

providing the first gate electrode and the second gate electrode from materials that are matched to each other in such a way that the first gate electrode and the second gate electrode form a diode structure.

Claim 14 (original): The method according to claim 13, which comprises:

applying an auxiliary layer between the ferroelectric layer and the first electrode layer; and

structuring the auxiliary layer when performing the step of structuring the ferroelectric layer and the first electrode layer.

Claim 15 (original): A method of producing a ferroelectric transistor according to claim 1, which comprises:

providing a semiconductor substrate with a surface;

applying, to the surface of the semiconductor substrate, a first gate intermediate layer, a ferroelectric layer, and a first electrode layer;

structuring the first electrode layer the ferroelectric layer, and the first electrode layer together to produce a first gate electrode;

producing a second gate intermediate layer disposed laterally relative to the first gate intermediate layer;

providing the second gate intermediate layer with a dielectric layer;

applying and structuring a second electrode layer to produce a second gate electrode adjacent and laterally overlapping the first gate electrode; and

providing the first gate electrode and the second gate electrode from materials that are matched to each other in such a way that the first gate electrode and the second gate electrode form a diode structure.

Claim 16 (original): The method according to claim 15, which comprises:

applying an auxiliary layer between the ferroelectric layer and the first electrode layer; and

structuring the auxiliary layer when performing the step of structuring the ferroelectric layer and the first electrode layer.